What is Claimed is:

1. A reset signal generating circuit comprising:

a power detector for maintaining the level of an applied voltage for a predetermined period;

a threshold voltage controller for outputting a voltage by regulating the level of a power voltage for generating a reset signal depending on variations of the power voltage and a bias voltage;

a feedback controller for pulling down an output voltage of the power detector when the power voltage reaches a predetermined level depending on an output voltage of the threshold voltage controller;

a pull-up controller for pulling up an output voltage of the power detector and outputting an output voltage variation of the power detector as the reset signal; and

a self-bias unit for outputting the bias voltage and regulating the amount of a current supplied from the threshold voltage controller to the feedback controller depending on variations of the power voltage.

2. The circuit according to claim 1, wherein the threshold voltage controller comprises:

a voltage driver for outputting a voltage depending

on variations of the power voltage to a predetermined level; and

a voltage pull-up unit for pulling up the output voltage of the threshold voltage controller to the level of the power voltage by outputting a voltage depending on variations of the power voltage when the power voltage reaches beyond the level of the bias voltage, depending on the variations of the power voltage and the bias voltage.

3. The circuit according to claim 2, wherein the voltage driver comprises a plurality of MOS transistors connected in series between a power voltage terminal and the feedback controller and having a gate connected in common to a drain.

4. The circuit according to claim 2, wherein the voltage pull-up unit comprises a plurality of PMOS transistors connected in series between a power voltage terminal and the feedback controller and having a gate connected in common to the self-bias unit.

5. The circuit according to claim 2, wherein the self-bias unit comprises a first NMOS transistor connected between the voltage pull-up unit and a ground voltage

terminal and having a gate connected in common to a source.

6. The circuit according to claim 5, wherein the self-bias unit further comprises a first switching device connected between the voltage pull-up unit and a ground voltage terminal and configured to turn on/off in response to an external control signal.

7. The circuit according to claim 2, wherein the self-bias unit is a diode having an input terminal connected to the voltage pull-up unit and an output terminal connected to a ground voltage terminal.

8. The circuit according to claim 7, wherein the self-bias unit further comprises a first switching device connected between the voltage pull-up unit and a ground voltage terminal and configured to turn on/off in response to an external control signal.

9. The circuit according to claim 2, wherein a bias voltage supplied to the voltage pull-up unit by the self-bias unit increases by a predetermined rate R,

wherein the R is represented by $R = CSC/(CSC + CST) \times VCC$ (CSC: whole capacitance of the self bias unit, CST:

coupling capacitance of the voltage pull-up unit, VCC: power voltage).

10. The circuit according to claim 1, wherein the feedback controller comprises:

a second NMOS transistor connected between an output node of the threshold voltage controller and a ground voltage terminal and having a gate connected to an output node of the power detector;

a third NMOS transistor connected between an output node of the power detector and a ground voltage terminal and having a gate connected to an output node of the threshold voltage controller; and

a first MOS capacitor having a drain and a source connected in common to an output node of the threshold voltage controller, and a gate connected to a ground voltage terminal.

11. The circuit according to claim 1, wherein the power detector comprises:

a power maintainer for maintaining and outputting the power voltage;

a second MOS capacitor for providing a ground voltage to the power maintainer at an initial stage of the

operation; and

a second switching device for selectively providing a ground voltage to the power maintainer depending on an output voltage of the power detector.

12. The circuit according to claim 1, wherein the pull-up controller comprises:

a first PMOS transistor having a drain and a source connected in common to a power voltage terminal, and a gate connected to an output node of the power detector;

a first inverter for inverting a signal of an output node of the power detector;

a second PMOS transistor connected between the power voltage terminal and an output node of the power detector and having a gate connected to an output terminal of the first inverter; and

a second inverter for inverting an output signal of the first inverter and outputting the inverted signal as a reset signal.

13. A nonvolatile ferroelectric memory device, comprising:

a reset generator for outputting a reset signal only when the power voltage is beyond a predetermined level

regardless of a power-up slope;

a reset transition detector for detecting a transition point of the reset signal and outputting a reset signal transition detecting signal;

an address latch for latching an address inputted through an address pad in response to a chip enable signal and an address transition control signal;

an address transition detector for detecting a transition point of an address outputted from the address latch and outputting an address transition detecting signal;

a chip enable transition detector for detecting transition points of the chip enable signal and the reset signal transition detecting signal and outputting a chip enable transition detecting signal; and

a synthesizer for synthesizing the address transition detecting signal and the chip enable signal transition detecting signal and outputting the synthesized signal.

14. The device according to claim 13, further comprising a buffer for receiving the chip enable signal through a chip enable pad and outputting the signal into the chip enable signal transition detector.

15. The device according to claim 13, further comprising a programmable circuit block including nonvolatile programmable code registers for programming inputs and outputs by using a reset signal transition detecting signal from the reset signal transition detector.

16. The device according to claim 13, wherein the reset signal generator comprises:

a power detector for maintaining the size of an applied voltage for a predetermined period;

a threshold voltage controller for regulating the level of the power voltage for generating a reset signal by regulating an output voltage depending on variations of the power voltage and a bias voltage;

a feedback controller for pulling down an output voltage of the power detector when the power voltage reaches a predetermined level depending on an output voltage of the threshold voltage controller;

a pull-up controller for pulling up an output voltage of the power detector and outputting a variation in an output voltage of the power detector as the reset signal; and

a self-bias unit for outputting the bias voltage and regulating the amount of a current supplied from the

threshold voltage controller to the feedback controller depending on variations of the power voltage.

17. The device according to claim 16, wherein the reset signal transition detector outputs the reset signal transition detecting signal having a pulse type when a reset operation is started.

18. The device according to claim 14, wherein the address latch unit receives and outputs an address while the chip enable signal and the address transition control signal are at disable states.

19. The device according to claim 18, wherein the address latch unit comprises:

a first selection latch unit for selectively latching an address inputted in response to a chip enable signal;

a second selection latch unit for selectively latching a signal outputted from the first selection latch unit in response to an address transition control signal; and

a buffer unit for buffering a signal outputted from the second selection latch unit and outputting the buffered signal.